DETAILED ACTION

1. This pertains to U.S. Application No. 10/595,567, filed 04/27/2006. Claims 1 – 8 are pending in this Application.

Specification

2. Applicants should include a statement prior to TECHNICAL FIELD (on Page 1 of the Specification) claiming benefit of Priority from a Japanese Patent Application.

Claim Objections

3. **Claims 1, 2, 3 and 7** are objected to because of the following issues:

- In claim 1 line 8, claim 3 line 6, and claim 7 line 7, delete "resisters" and insert --registers--.
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- In claims 1 and 7, there is no antecedent bases for "the first logic circuit".
- In claim 2, line 5, delete "circuits" and insert --circuit--; claim 2, there is no antecedent basis for "fourth logic circuits"

4. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 1 – 8** are generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. Examples can be

found in claims 1, 3 and 7: "external data is written in a first latching firstly after the external data is input" and ""external data is not written in a second latching firstly after the external data is input"); in claims 2, 4 and 8: "data input to each of the second logic circuits is not written in a fourth latching firstly after the data being input"; and in claim 5: "first group of registers is constituted by a register to which the external data is directly input". Applicants should very carefully review the claim language to correct these and other deficiencies. It is very difficult to understand these claimed limitations, as described.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3, 5, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,678,645 B1 to Rajsuman et al. (hereinafter, "Rajsuman"), in view of U.S. Patent No. 7,062,739 B2 to Monthie et al. (hereinafter, "Monthie").

9. **Referring to claims 1, 3 and 7**, Rajsuman teaches a design method of an iC (claim 1 – see Rajsuman , col. 1, ll. 6 - 13), an IC (claim 3 - see Rajsuman, Fig. 5), and a design tool (apparatus) of an IC (claim 7 - see Rajsuman, col. 1, ll. 6 – 13), wherein the IC comprises a plurality of logic blocks (i.e., cores or macros - see Rajsuman, col. 1, ll. 16 - 28) comprises: (a) first logic circuits to which external data is written using a

control circuit (Rajsuman teaches independent cores that can be accessed separately using glue logic and arbitration before integration of the individual cores into an SoC – see Rajsuman, col. 5, ll. 16 – 30; col. 6, ll. 27 – 33; col. 7, line 60 – col. 8, line 5); (b) second logic circuits to which external data is not written into and a control circuit for controlling the data in accordance with the output signal from the first logic circuit (see again item (a) above); wherein the design method comprises the steps of: first designing layout and timing verification of the first logic circuits/control lines/data lines between the logic blocks (see col. 5, ll. 16 – 48) and second designing layout and timing verification of one of the second logic circuits (see again col. 5, ll. 16 - 48; col. 11, ll. 30 - 52).

Although Rajsuman teaches including independent core blocks in his invention, he does not specifically refer to group of registers for writing data into, in his invention. However, Monthie discloses a gate reuse methodology for diffused cell – based IP blocks that teaches including a group of registers at the I/O interface of an IC (see Monthie – Figs. 2 and 3; col. 2, ll. 37 – 63). Since using data registers are now commonly used at the I/O interfaces of complex macro/core blocks in order to control the I/O specifications of these blocks for possible integration in an SoC design, it would therefore be obvious to a person of ordinary skill in the art at the time off the invention to modify the teachings of Rajsuman with the teachings of Monthie to include groups of registers for data writing into individual logic blocks for independent logic verification of each block.

10. **As per claim 5**, see again Monthie - Figs. 2 and 3; col. 3, ll. 52 – 64, which teach the group of registers with direct access to external data, as claimed.

11. **As per claim 6**, see Rajsuman – col. 2, line 63 – col. 3, line 30, which teach the claimed limitations pertaining to adjusting the timing of the control signal for each core.

Allowable Subject Matter

12. **Claims 2, 4 and 8** would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: prior art does not teach, or fairly suggest, the additional claimed limitations pertaining the third and fourth logic circuits/group of registers and the third and fourth design steps/timing verification.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAGID Y. DIMYAN whose telephone number is (571)272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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07 April 2008

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